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59

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,225	10/22/2003	Lee Doyle Whetsel	TI-14124D.6	3588

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,225	WHETSEL, LEE DOYLE	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 25-51 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 25-28,31,34-44 and 46-51 is/are rejected.

7)☒ Claim(s) 29,30,32,33 and 45 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/22/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 are cancelled.

Claims 25-51 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on October 22, 2003 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

The examiner would like to point out that although applicant has discussed numerous US patents, none of the discussed US patents are listed on the form1449. The examiner requests applicant to submit another form 1449 listing all US references discussed in applicant's remarks in Preliminary Amendment A pages 30-35.

Drawings

The drawings were received on October 20, 2003. These drawings are acceptable.

Specification

The preliminary amendment submitted on October 22, 2003 which modifies the Title, Specification and the Claims, has been entered prior to examination.

Allowable Subject Matter

Claims 29 30, 32, 33, 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 25-51 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 25, of copending

Application No. 10/649274. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 25 of application 10/649274 states;

An integrated circuit comprising:

A. a substrate;

B. operating circuits formed on the substrate, the operating circuits including an operating bus of plural leads for carrying normal operating signals;

C. a serial data input lead formed on the substrate, a serial data output lead formed on the substrate, and a plurality of serial scan paths, each formed of scan registers, formed on the substrate and coupled between the serial data input lead and the serial data output lead, the serial scan paths for carrying serial data signals, including command signals, an expected data pattern signal, and a protocol selection signal, on the substrate,

i. one of the plurality of serial scan paths including a data register having plural data storage locations, a serial input coupled between the serial data input lead and the data storage locations for carrying serial data signals to the data storage locations, a serial output coupled between the serial data output lead and the data storage locations for carrying signals out of the data storage locations, data inputs coupled between the data storage locations and the operating bus for carrying the normal operating signals to the data storage locations, and a control input, and

ii. another of the plurality of serial scan paths including a command register, the command register having plural command storage locations for storing command signals, a control input, a serial input coupled between the serial data input lead and the command storage locations for carrying the command signals to the storage locations, and a serial output coupled to the serial data output lead;

D. an expected data memory formed on the substrate, the expected data memory having plural expected data pattern storage locations for storing an expected data pattern signals and having at least one input coupled between one of the serial scan paths and the expected data storage locations for receiving the expected data pattern signals from the serial scan path;

E. a comparator formed on the substrate, the comparator having first inputs coupled to the operating bus and second inputs coupled to the expected data memory for comparing at least some of the normal operating signals to corresponding ones of the expected data pattern signals, the comparator having a compare output lead;

F. a mode select input lead formed on the substrate, the mode select input lead for carrying a mode select signal;

G. a serial data clock input lead formed on the substrate, the serial data clock input lead for carrying a serial data clock signal;

H. an access port formed on the substrate, the access port including control circuitry and having a plurality of control outputs, at least one first control output coupled to the control input of the command register, at least one second control output coupled

to the control input of the data register, a first input coupled to the mode select input lead and a second input coupled to the serial data clock input lead, the control circuitry being operable selectively to control shifting of the serial data signals between the serial data input lead and the serial data output lead, and into and out of the command register, and into and out of the data register responsive to the mode select signal and the serial data clock signal;

J. a protocol selection memory having at least one storage location for storing a protocol selection signal, and an input coupled to one of the serial scan paths, the protocol selection memory storage location for receiving the protocol selection signal from the serial scan path; and

K. an event control circuit including a protocol input coupled to the protocol selection memory, an event input lead coupled to the compare output lead, and an event output lead.

Independent claims 25, 26, and 27 recite features such as; operating circuits; an expected data memory coupled to serial data input lead; a comparator having first inputs coupled to the operating circuits and second inputs coupled to the expected data memory; data register coupled to the first inputs of the comparator, to the serial data input lead, and to serial data output lead; a mode select input lead; a serial data clock input lead; and an access port. These elements are either formed on a substrate or are permanently integrated together. Claims 25 and 26 further recite a command register.

Claim 25 of the copending application (listed above) recites in varying degrees of details all of the above features.

As per claim 28, claim 25 of the copending application (listed above) recites control circuitry and having a plurality of control outputs, at least one first control output coupled to the control input of the command register, at least one second control output coupled to the control input of the data register, a first input coupled to the mode select input lead and a second input coupled to the serial data clock input lead, the control circuitry being operable selectively to control shifting of the serial data signals between the serial data input lead and the serial data output lead, and into and out of the command register, and into and out of the data register responsive to the mode select signal and the serial data clock signal;

As per claims 31, 41, and 47, claim 25 of the copending application (listed above) recites the claimed bus in B, C, and E.

As per claims 34-36, claim 25 of the copending application (listed above) recites, the claimed features of selection circuitry and clocks and registers, in G, J, and K.

As per claim 37-40, claim 25 of the copending application (listed above) recites, the claimed features of the comparator circuitry, match signals and expected data memory in C, D, E, H and claim 40 of the copending application.

As per claims 42-44, 46, and 48-49, the copending application addresses the comparator expected data memory in claims 25, 34, 35, and 40.

As per claim 50, claim 25 of the copending application (listed above) recites the claimed features in G, J, and K.

As per claim 51, claim 25 D of the copending application (listed above) recites an expected data memory formed on the substrate, the expected data memory having plural expected data pattern storage locations for storing an expected data pattern signals and having at least one input coupled between one of the serial scan paths and the expected data storage locations for receiving the expected data pattern signals from the serial scan path.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

GUY LAMARRE
PRIMARY EXAMINER